

**AMENDMENTS TO THE CLAIMS:**

1. (original) An improved p-type gallium nitride-based semiconductor device comprising:

a device structure that includes at least one p-type Group III nitride layer that includes some gallium;

a first silicon dioxide layer on said p-type layer;

a layer of a Group II metal source composition on said first SiO<sub>2</sub> layer; and

a second SiO<sub>2</sub> layer on said Group II metal source composition layer.

2. (currently amended) A semiconductor device according to Claim 1 wherein said device structure comprises:

a conductive silicon carbide substrate;

a conductive buffer layer on said silicon carbide substrate for providing a crystal transition between said substrate and said Group III nitride portions of said device; and

an n-type Group III nitride layer on said buffer layer,

wherein said p-type Group III nitride layer is adjacent said n-type Group III nitride layer to form a p-n junction.

3. (original) A device according to Claim 1 wherein said first silicon dioxide layer is thick enough to create vacancies to a depth in said p-type layer that encourages atoms of said Group II metal to diffuse thereto while still permitting diffusion from said Group II metal source composition through said first SiO<sub>2</sub> layer and into said p-type layer.

4. (original) A device according to Claim 1 wherein:

said first SiO<sub>2</sub> layer is about 1000 Å thick;

said Group II metal source composition layer is about 1000 Å thick; and

said second SiO<sub>2</sub> layer is about 2500 Å thick.

5. (original) A device according to Claim 1 wherein said Group III nitride comprises GaN and said source composition layer is selected from the group consisting of magnesium and zinc.

6. (cancelled)

7. (previously amended) A device structure according to Claim 2 wherein said substrate is n-type and has a carrier concentration of between about  $1 \times 10^{16}$  cm<sup>-3</sup> and about  $1 \times 10^{19}$  cm<sup>-3</sup>.

8. (original) A device according to Claim 1 wherein said Group II metal source composition layer comprises a Group II metal-containing compound.

9. (original) A device according to Claim 8 wherein said compound is selected from the group consisting of magnesium nitride and zinc phosphide.

10. (previously amended) A device according to Claim 1 wherein said p-type gallium nitride layer has the formula  $\text{Ga}_x\text{Al}_y\text{In}_{1-x-y}\text{N}$  where  $0 < x \leq 1$  and  $0 \leq y \leq 1$ .

11. (original) A device according to Claim 1 comprising a plurality of silicon dioxide portions on said p-type Group III nitride layer, with a respective portion of said source composition on each said silicon dioxide portion.

12. (previously amended) An improved p-type gallium nitride-based semiconductor device comprising:

a device structure that includes at least one p-type Group III nitride layer that includes some gallium;

a plurality of silicon dioxide portions on said p-type Group III nitride layer;  
a portion of a Group II metal source composition layer on each of said silicon dioxide portions; and  
a second silicon dioxide layer on said Group II metal source composition layer,  
wherein said second silicon dioxide layer is limited to said source composition layer portions.

13. (original) A device according to Claim 11 wherein said second silicon dioxide portion covers said source composition portions and portions of said p-type Group III nitride layer.

14. (currently amended) An improved p-type gallium nitride-based device comprising:  
a conductive silicon carbide substrate;  
a conductive buffer layer on said silicon carbide substrate for providing a crystal transition between said substrate and said GaN portions of said device;  
an n-type GaN layer on said buffer layer;  
a p-type GaN layer adjacent on said n-type layer and forms a p-n junction;  
a first silicon dioxide layer on said p-type layer;  
a magnesium layer on said first SiO<sub>2</sub> layer for supplying p-type dopant to said p-type layer; and  
a second SiO<sub>2</sub> layer on said Mg layer for passivating said device;  
said first silicon dioxide layer being thick enough to create vacancies to a required depth in said p-GaN layer when said device is heated to temperatures between about 750° and 950° C while still permitting diffusion from the magnesium layer through said first SiO<sub>2</sub> layer and into the p-GaN layer at such temperatures.

15. (original) A device according to Claim 14 wherein said substrate is n-type.

16. (original) A device according to Claim 14 wherein said buffer is selected from the group consisting of: graded layers of Group III nitrides, homogeneous layers of Group III nitrides, heterogeneous layers of Group III nitrides and combinations thereof.

17. (original) A device according to Claim 14 wherein said n-type layer comprises  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  where  $0 \leq x \leq 1$  and  $0 \leq y \leq 1$

18. (previously amended) A device according to Claim 14 wherein said p-type layer comprises  $\text{Ga}_x\text{Al}_{1-x}\text{N}$  where  $0 < x \leq 1$  and  $0 \leq y \leq 1$ .

19-44. (cancelled)

Please add the following new claims:

45. (new) An improved p-type gallium nitride-based semiconductor device comprising:

a conductive silicon carbide substrate;  
a conductive buffer layer on said silicon carbide substrate for providing a crystal transition between said substrate and Group III nitride portions of said device;  
an n-type Group III nitride layer on said buffer layer;  
a p-type Group III nitride layer that includes some gallium directly on said n-type layer and forms a p-n junction;  
a first silicon dioxide layer on said p-type layer;  
a layer of a Group II metal source composition on said first  $\text{SiO}_2$  layer; and  
a second  $\text{SiO}_2$  layer on said Group II metal source composition layer.

46. (new) A semiconductor device according to Claim 45, wherein said layer of a Group II metal source composition comprises magnesium.

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47. (new) A semiconductor device according to Claim 46, comprising a plurality of silicon dioxide portions on said p-type Group III nitride layer, with a respective portion of said magnesium source composition on each said silicon dioxide portion.

48. (new) A semiconductor device according to Claim 47, comprising:  
a plurality of silicon dioxide portions on said p-type Group III nitride layer;  
a portion of said magnesium source composition layer on each of said silicon dioxide portions; and  
a second silicon dioxide layer on said magnesium source composition layer,  
wherein said second silicon dioxide layer is limited to said magnesium source composition layer portions.

49. (new) A semiconductor device according to Claim 47, wherein said second silicon dioxide portion covers said magnesium source composition portions and portions of said p-type Group III nitride layer.